

Amendments to the Specification:

Please insert the following paragraph at page 1, between lines 5 and 6:

This application is based upon and claims the benefit of priority from the prior Japanese Patent Application Nos. 8-035247, filed February 22, 1996; 8-222564, filed August 23, 1996; 8-235617, filed September 5, 1996; and 9-047327, filed February 14, 1997, and from U.S. Application Nos. 09/975,150, filed October 12, 2001; 09/166,42, filed on October 5, 1998; and 08/804,069, filed on February 21, 1997, the entire contents of which are incorporated herein by reference.

Please replace the paragraph beginning on page 21, lines 7-20, with the following amended paragraph:

The program then proceeds to step S3, at which the CPU 8 reads out the image data written in the line memory 4, temporarily registers the image data into the RAM 9 included in the CPU 8, and carries out an operation defined by Equation 1 given below to determine a phase-related index $V_1(\Phi)$:

$$V_1(\Phi) = \sum_{i=0}^{Nd-2} \{PD(i+1) - PD(i)\}^2 \quad (2)$$

wherein $PD(i)$ denotes image data (also referred to as pixel data) at an i -th address (or pixel position); Nd denotes the factor in the PLL circuit 7 (that is, the total number of pixels included in one line); and Φ denotes a delay in the delay circuit 10. It should be noted that $PD(i+1)$ and $PD(i)$ depend on the delay Φ in the delay circuit 10. Namely the phase-related index $V_1(\Phi)$ defined by Equation 1 is the sum of the squared differences between image data at adjoining pixel positions on the same line. This value indicates the relationship between the phase of the analog video signal 101 and the phase of the dot clock 201 and is thereby

called 'phase-related index'. The value of the phase-related index $V_1(\Phi)$ depends upon the delay Φ in the delay circuit 10.

Please replace the paragraph beginning on page 43, lines 15-23, with the following amended paragraph:

In the above procedure, the video signal 101 representing an effective signal area of 800 pixels has been sampled by the dot clock generated with the provisional factor N_k ; the sampled image data have been written into the line memory 4; and the starting address AD_s and the terminal address AD_t of the effective signal area have been detected based on the image data read out of the line memory 4. The width of the effective signal area can be calculated to be $(A_e - A_s + 1)$ $(AD_t - AD_s + 1)$ pixels from these addresses AD_s and AD_t . Note that the true width of the effective signal area for this video signal is known to be 800 pixels.